UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,713	04/15/2004	Glenn A. Baxter	X-1641-2 US	6785

24309 7590 10/05/2006

XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
SHIN, CHRISTOPHER B	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,713	BAXTER ET AL.	
	Examiner	Art Unit	
	Christopher B. Shin	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-36 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-36 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 2 sheets.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pham et al. (6,212,593).

a. The Pham reference teaches the claimed limitations as follows:

Claims 1-8, 11-32, 35 Pham (6,212,593)

- Apparatus for controlling direct access to memory circuitry by a device, comprising
  - System of figure 1A, (172)
- A streaming interface configured to transmit and receive a communication sequence to and from said device
  - Figure 1A, (146, 164)
- Control logic configured to implement a plurality of DMA engines configured to read and write data to and from said memory circuitry
  - Figure 1A, 2, (150, 178)
- A set of registers configured to store control data fro said plurality of DMA engines
  - Feature of figures 5A & 5B
- Wherein communication sequence comprises a header, a data section, and footer
  - Feature communication protocols can used in the system of figure 1, see column 1, lines 40-65, column 3, line 66
- Wherein at least one of said header and said footer includes at least a portion of said control data

- Feature communication protocols can used in the system of figure 1, see column 1, lines 40-65, column 3, line 66

- Wherein each of said plurality of DMA engines is configured to read and write said data by processing at least one chain of descriptors, each said at least one chain having at least one descriptor
  - Feature of column 13, lines 25-52, figures 7-8
- Wherein said set of registers comprises, for each of said plurality of DMA engines: a current descriptor register configured to store a pointer to a descriptor currently processed
  - Feature of figure 5A & 5B
- A next descriptor register configured to store a pointer to a descriptor subsequently processed
  - Feature of figure 5A & 5B
- A current address register configured to store an address in said memory circuitry associated wit a read or write transaction
  - Feature of figure 5A & 5B
- A current length register configured to store a length of data to be read from or written to said memory circuitry
  - Feature of figure 5A & 5B

- Wherein each of said plurality of DMA engines is configured to read or write data in response to said current descriptor register receiving a value
  - Feature of figure 5A & 5B
- Wherein said set of registers comprises, for each of said plurality of DMA engines: a Status register for storing one or more status flags
  - Feature of figure 5A & 5B
- Wherein said set of registers includes an interrupt register, and wherein said control logic is configured to generate an interrupt signal in response to information stored in said interrupt register
  - Feature of figure 5A & 5B
- Wherein said DMA controller is disposed within an integrated circuit
  - Feature of 1B

b. The main difference between the claimed invention and the teachings of the Pham reference is that the Pham does not expressly disclose the claimed "communication sequence"; however, the Pham does teach a DMA unit with substantially identical function/operation of the claimed invention. Therefore, it

would have been obvious at the time the invention was made to one skilled in the art to easily come up with the invention (i.e., system and method) from the substantially identical teachings of the Pham reference.

c. As for claims 9-10, 33-34, further add limitation regarding the claimed memory being DDR/SDRAM; however, one skilled in the art can easily substitute memory with different types of memory such as DDR/SDRAM for a faster speed. This is because DDR/SDRAM is commonly used with DMA for faster memory access speed. The examiner takes official notice on such practice.

d. As for claims 36, further ad limitation regarding of implementing using programmable logic device. This is well known and commonly practiced implementation in the art. The examiner takes official notice on such practice.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher B. Shin whose telephone number is 571-272-4159. The examiner can normally be reached on 6:30-5:00 M,Tu,Th,F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on 571-272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CHRISTOPHER SHIN
PRIMARY EXAMINER
OF 2181

September 27, 2006
cbs